DESCRIPTION

The following specifications are applied to the following IPS-Pro-TFT LCD module.

Product Name : VVX32H101G00

Product Factory : Panasonic Liquid Crystal Display Co.,Ltd. (Mobara/Utsunomiya/Himeji, Japan)
Panasonic Liquid Crystal Display Czech,s.r.o. (Czech Republic)
Panasonic Liquid Crystal Display Malaysia Sdn.Bhd. (Malaysia)

General Specifications

Effective display area	: (H) 697.685 × (V) 392.256	(mm)
Number of pixels	: (H) 1,366 × (V) 768	(pixels)
Pixel pitch	: (H) 0.51075 × (V) 0.51075	(mm)
Color pixel arrangement	: R+G+B vertical stripe	
Display mode	: Transmissive mode Normally black mode	
Top polarizer type	: Semi-Glare	
Number of colors	:16,777,216	(colors)
Viewing angle range	: wide version (Horizontal & Vertical : 178° at φ=0°,90°,180°,270°, CR≧10)	
Input signal	: mini LVDS (LVDS : Low voltage differential signaling)	
Backlight	: 72 tips of LED (LED: Light-emiting diode)	
External dimensions	: Typ. (H) 735.4 × (V) 433.0 × (t) 37.0	(mm)
Weight	: Typ. (6,000)	(g)

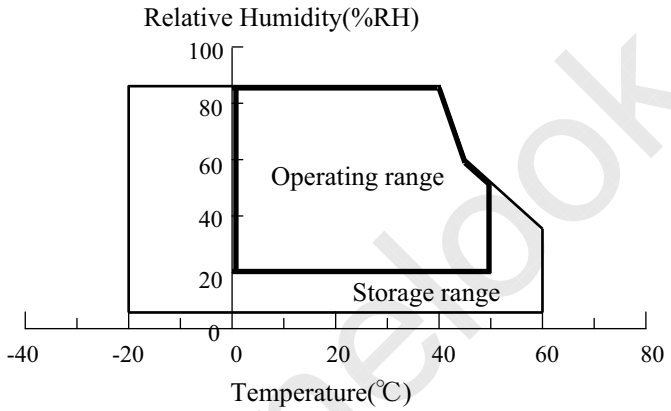
1. ABSOLUTE MAXIMUM RATINGS

1. 1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		UNIT	NOTE
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	℃	1),5),6)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5 G)	-	14.7(1.5 G)	m/s^2	3)
Shock	-	29.4(3 G)	-	294(30 G)	m/s^2	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illumination at LCD Surface	-	50,000	-	50,000	1x	

Note 1) Temperature and Humidity should be applied to the glass surface of a IPS-Pro TFT LCD module, not to the system installed with a module.

2) Ta≦40 ℃ · · · · · · Relative humidity should be less than 85 %RH max. Dew is prohibited.
Ta＞40 ℃ · · · · · · Relative humidity should be lower than the moisture of the 85 %RH at 40 ℃.



3) Frequency of the vibration is between 15 Hz and 100 Hz. (Remove the resonance point) 1 hour.
4) Direction : ±X, ±Y, ±Z (One time each direction)
5) Pulse width of the shock is 10 ms.
6) The temperature of LCD front surface would be 65 ℃ in operating, it may affect the optical characteristics however it does not damage the function of the module.

1. 2 Electrical Absolute Maximum Ratings

(1)TFT-LCD module V_{SS} = 0 V

ITEM	SYMBOL	Min.	Max.	UNIT	NOTE
Source Driver Analog Power Supply	AVDD	0	16.0	V	
Driver Logic Power Supply	VDD	0	4.0	V	
Gate Driver Power Supply	VON	0	37	V	
	VON-VOFF	0	44	V	
Gate Driver Ground	VOFF	-20	0.3	V	
Gamma Corrected Power Supply	VREF1～6	0.4AVDD	AVDD+0.3	V	
Gamma Corrected Power Supply	VREF8～12	-0.3	0.6AVDD	V	
Common Plate Power Supply	VCOM	VCOMaj - 2.0	VCOMaj + 2.0	V	5)
Input Voltage for logic	V_1	-0.3	VDD + 0.3	V	1)
	V_2	-0.3	VDD + 1.2	V	6)
	V_3	-0.3	7	V	7)
Electrostatic Durability	V_{ESD0}	±100		V	2),3)
	V_{ESD1}	±20		kV	2),4)

Note 1) It is applied to pixel data signal, clock signal and other control signals.
2) Discharge Coefficient : 250 pF - 100 Ω, Environmental : 25 ℃ - 70%RH
3) It is applied to I/F connector pins.
4) It is applied to the surface of a metallic bezel and a LCD panel.
5) VCOMaj means adjusted VCOM voltage.
6) It is applied to SDA, SCL signal.
7) It is applied to WP signal.

(2) Backlight unit

ITEM	SYMBOL	Max.	UNIT	NOTE
Temperature Junction of LED	Tj	100	℃	1)
Forward Current	If	720	mA	2)

Note 1) The specification shall be applied to each LED.
2) The specification shall be applied at connector pins for LED at start-up.

2. INITIAL OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted.

The optical characteristics should be measured in a dark room or equivalent state.

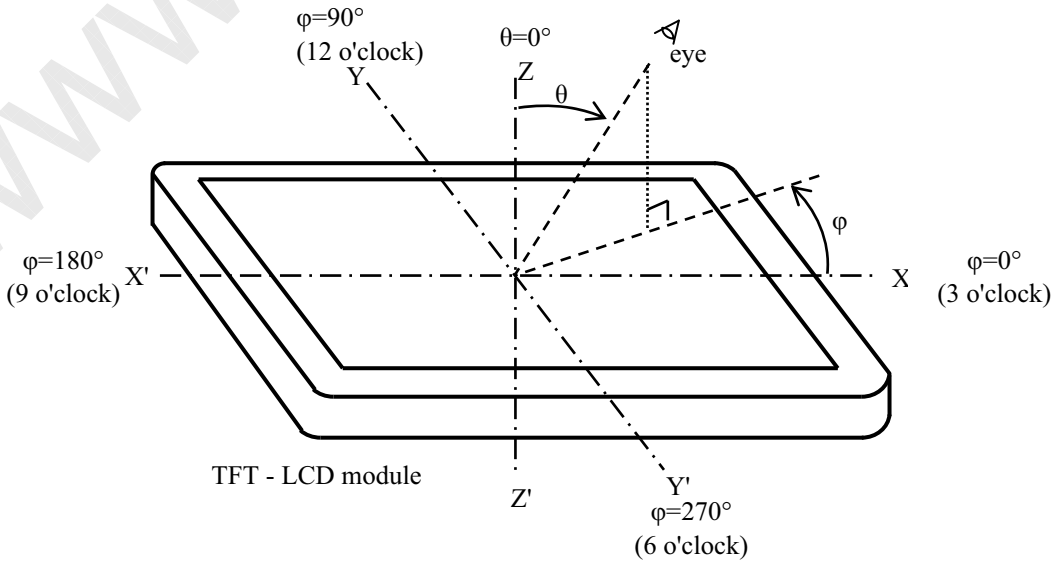
Measuring equipment : CS-1000A, or equivalent

Ambient Temperature =25 ℃ , V_{DD}=12.0 V , f V=60 Hz ,

I_L=12mArms (on duty 100%)

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast ratio		CR	θ= 0 ° 1)	800	1400	-	-	2)
Response time	Rise	ton		-	10	20	ms	3)
	Fall	toff		-	8	20	ms	3)
Brightness of white		Bwh		350	450	-	cd/m^2	
Brightness uniformity		Buni		-	-	40	%	4)
Color chromaticity (CIE)	Red	x		0.560	0.590	0.620	-	【Gray scale =255】
		y		0.305	0.335	0.365		
	Green	x		0.310	0.340	0.370		
		y		0.570	0.600	0.630		
	Blue	x		0.125	0.155	0.185		
		y		0.035	0.065	0.095		
	White	x		0.250	0.280	0.310		
		y		0.253	0.283	0.313		
Variation of color position (CIE)	Red	Δx	θ= 50 ° φ= 0 °, 90 °, 180 °, 270 ° 1)	-	-	0.04	-	5) 【Gray scale =255】
		Δy		-	-	0.04		
	Green	Δx		-	-	0.04		
		Δy		-	-	0.04		
	Blue	Δx		-	-	0.04		
		Δy		-	-	0.04		
	White	Δx		-	-	0.04		
		Δy		-	-	0.04		
Contrast ratio at 89 °		CR89	φ=0°,90°, 180°,270° 6)	10	-	-	-	Estimated value
Image sticking		-	Mosaic pattern	Invisible			-	7)

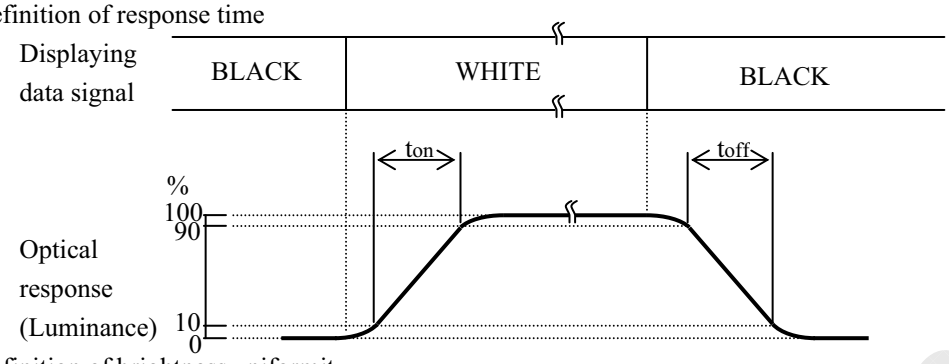
Note 1) Definition of viewing angle



Note 2) Definition of contrast ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of response time



4) Definition of brightness uniformity

Display pattern is white (255 level) . The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

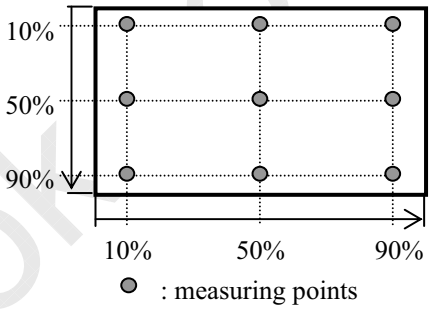
$$B_{uni} = \frac{\left| B_{max} \text{ or } B_{min} - B_{ave} \right|}{B_{ave}} \times 100$$

where, B_{max} = Maximum brightness

B_{min} = Minimum brightness

B_{ave} = Average brightness

$$B_{ave} = \frac{\sum_{k=1}^{9} (B(k))}{9}$$



5) Variation of color position on CIE

Variation of color position on CIE is defined as difference between colors at θ= 0° and at θ= 50°& φ= 0°, 90°, 180°, 270°.

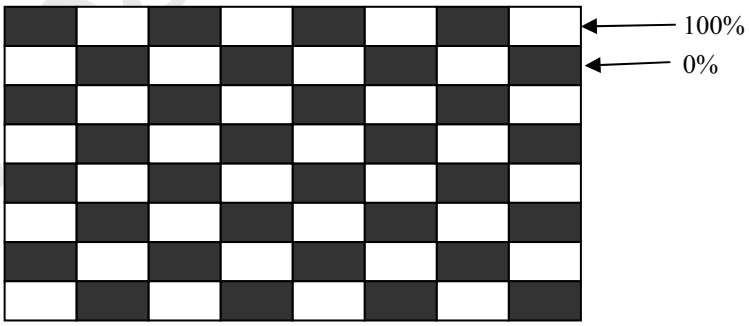
6) Contrast ratio at 89 °

Evaluetion conditions are on horizontal & vertical axis

7) Image sticking

Condition : Operating mosaic pattern for 2 hours and gray scale (22 %) for 1 hour.

Mosaic pattern



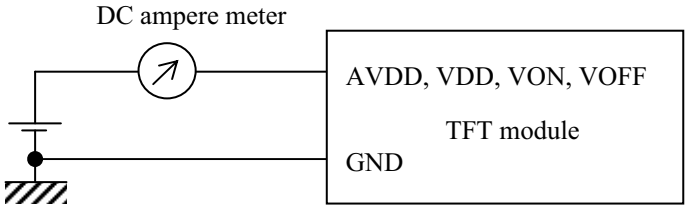
3. ELECTRICAL CHARACTERISTICS

3. 1 TFT-LCD module

Ta = 25 ℃ , GND = 0 V

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Source Driver Analog Power Supply Voltage	AVDD	12.286	12.586	12.886	V	
Ripple voltage of AVDD	Vrip_avdd	-	-	350	mV	5), 6)
		-	-	250	mV	5), 8)
Driver Logic Power Supply Voltage	VDD	2.4	2.5	2.6	V	
Ripple voltage of VDD	Vrip_vdd	-	-	150	mV	5), 6)
Gate Driver Power Supply Voltage	VON	29.0	30.5	32.5	V	
Ripple voltage of VON	Vrip_von	-	-	500	mV	5), 6)
Gate Driver Ground Voltage	VOFF	-6.35	-5.8	-5.25	V	
Ripple voltage of VOFF	Vrip_voff	-	-	200	mV	5), 6)
Input High Voltage for logic	VIH1	0.8VDD	-	VDD	V	2)
Input Low Voltage for logic	VIL1	0	-	0.2VDD	V	2)
Input High Voltage for EEPROM	VIH2	0.8VDD	-	VDD+1.2	V	3)
	VIH3	0.8VDD	-	5.25	V	7)
Input Low Voltage for EEPROM	VIL2	0	-	0.2VDD	V	3)
Output Low Voltage from EEPROM	VOL	-	-	0.4	V	4)
Common Plate Voltage	VCOM	-	5.125	-	V	
Ripple voltage of VCOM	Vrip_vcom	-	-	200	mV	5), 6)
Source Driver Analog Power Supply Current	IADD	-	150	200	mA	1)
Driver Logic Power Supply Current	IDD	-	20	30	mA	1)
Gate Driver Power Supply Current	ION	-	3.0	5.0	mA	1)
Gate Driver Ground Current	IOFF	-5.0	-3.0	-	mA	1)
Gamma Corrected Power Supply Voltage 1	VREF1	-	12.033	-	V	
Gamma Corrected Power Supply Voltage 2	VREF2	-	10.656	-	V	
Gamma Corrected Power Supply Voltage 3	VREF3	-	9.329	-	V	
Gamma Corrected Power Supply Voltage 4	VREF4	-	8.690	-	V	
Gamma Corrected Power Supply Voltage 5	VREF5	-	8.161	-	V	
Gamma Corrected Power Supply Voltage 6	VREF6	-	6.342	-	V	
Gamma Corrected Power Supply Voltage 8	VREF8	-	4.462	-	V	
Gamma Corrected Power Supply Voltage 9	VREF9	-	3.921	-	V	
Gamma Corrected Power Supply Voltage 10	VREF10	-	3.257	-	V	
Gamma Corrected Power Supply Voltage 11	VREF11	-	1.893	-	V	
Gamma Corrected Power Supply Voltage 12	VREF12	-	0.479	-	V	
Ripple voltage of VREF	Vrip_VREF	-	-	200	mV	5), 6)

Note 1) fV=60.0Hz, fCLK=156MHz, each power supply voltage is typical condition and display pattern is white raster.



2) It is applied to LP, POLR, POLL, CPV, DATA1 and DATA2 signal.
3) It is applied to SDA, SCL signal.
4) It is applied to SDA signal. IOL=1.5mA
5) The above specification is defined at connector CN1.
6) Display pattern is white raster.
7) It is applied to WP signal.
8) Display pattern is 128gray raster.

3. 2 Backlight unit

ITEM		SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Forward Currnet (One LED Assembly)	Anode	Ifa	228	240	252	mA	
	Cathode	Ifc	114	120	126	mA	
Forward Voltage	String	Vf	57.6	61.2	64.8	V	
	Variation	Vf(unit)	-	-	(1.5)	V	One BL unit
Power Consumption		Pbl	26.3	29.4	34.5	W	
PWM	Duty	PD	0	-	100	%	
	Frequency	PF	95	-	182	Hz	One BL unit
LED Life time		-	30000	-	-	h	(2)

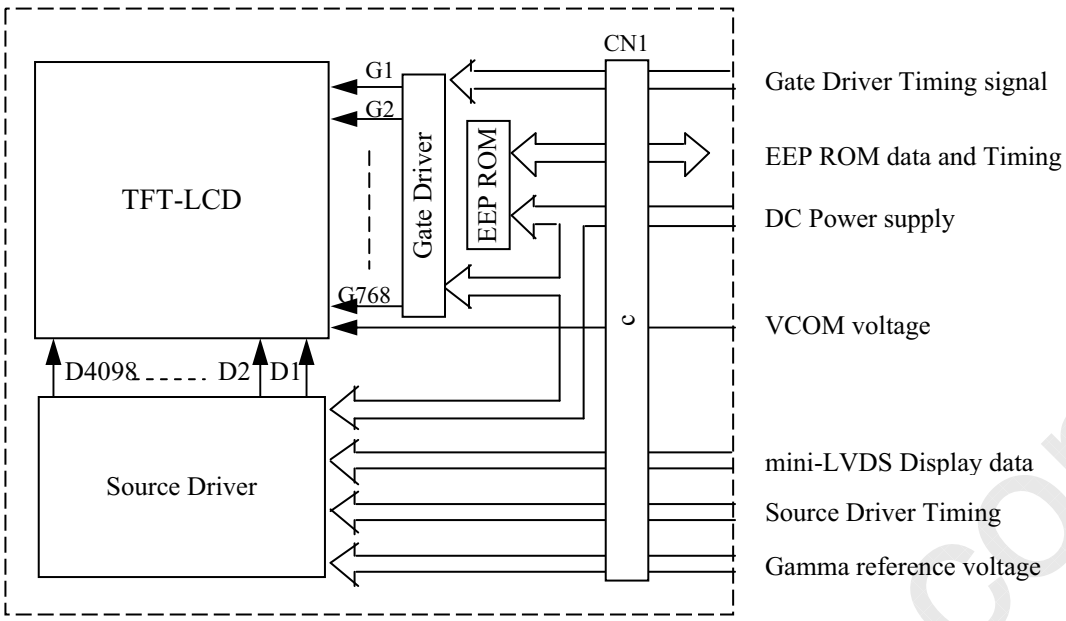
One Backlight Unit : 2 LED Array
One LED Array : 2 LED String
One LED String : 18 LED package

Note 1) This characteristics should be applied putting on the LED about 60 minutes later with ambient temperature. (Ta = 25 ℃ ± 2 ℃)

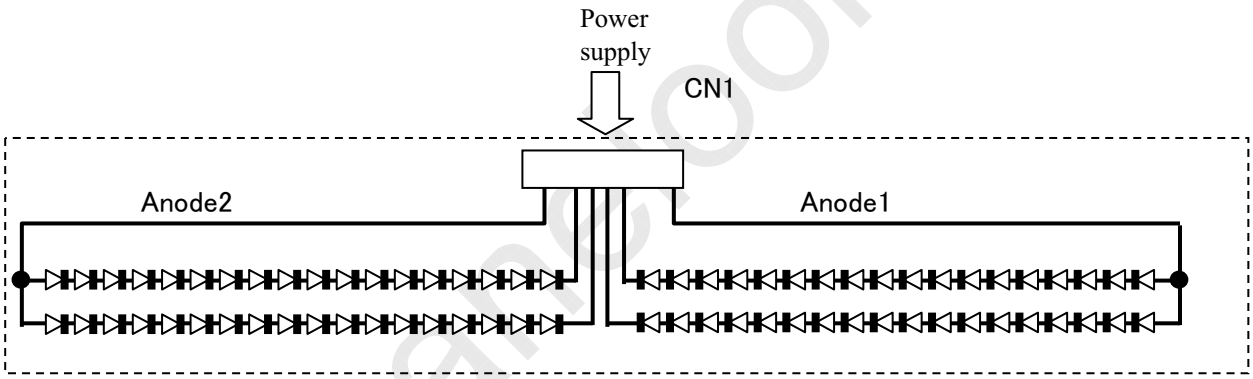
2) Life time of a LED is defined as follows. The life is determined as the time at which brightness of the LED is 50 % compared to that of initial value at that typical forward current on condition of continuous operating at 25 ± 2 ℃.

4. BLOCK DIAGRAM

4. 1 TFT-LCD module



4. 2 Backlight unit



5. INTERFACE PIN ASSIGNMENT

5. 1 TFT-LCD module

CN1:MOLEX 503366-6011

PIN No.	SYMBOL	DESCRIPTION	NOTE
1	GND	Ground(0V)	3)
2	SCL	I2C-bus Serial Clock	
3	SDA	I2C-bus Serial Data	7)
4	WP	EEPROM Write Protect	6)
5	VREF12	Gamma Corrected Power Supply	
6	VREF11		
7	VREF10		
8	VREF9		
9	VREF8		
10	VCOM	Common Plate Power Supply	
11	VCOM		
12	AVDD	Sourcr Driver Analog Power Supply	1)
13	AVDD		
14	AVDD		
15	AVDD		
16	GND	Ground(0V)	3)
17	VDD	EEPROM Power Supply	2)
18	VDD	Driver Logic Power Supply	2)
19	VDD		
20	LP	Latch Clock Input	
21	POL	Polarity Control Input	
22	GND	Ground(0V)	3)
23	CLKL-	Pixel Clock (Left Side)	5)
24	CLKL+		
25	GND	Ground(0V)	3)
26	LV2L-	mini-LVDS Pixel Data (Left Side)	5)
27	LV2L+		
28	GND	Ground(0V)	3)
29	LV1L-	mini-LVDS Pixel Data (Left Side)	5)
30	LV1L+		

PIN No.	SYMBOL	DESCRIPTION	NOTE
31	GND	Ground(0V)	3)
32	LV0L-	mini-LVDS Pixel Data (Left Side)	5)
33	LV0L+		
34	GND	Ground(0V)	3)
35	CLKR-	Pixel Clock (Right Side)	5)
36	CLKR+		
37	GND	Ground(0V)	3)
38	LV2R-	mini-LVDS Pixel Data (Right Side)	5)
39	LV2R+		
40	GND	Ground(0V)	3)
41	LV1R-	mini-LVDS Pixel Data (Right Side)	5)
42	LV1R+		
43	GND	Ground(0V)	3)
44	LV0R-	mini-LVDS Pixel Data (Right Side)	5)
45	LV0R+		
46	GND	Ground(0V)	3)
47	VREF6	Gamma Corrected Power Supply	
48	VREF5		
49	VREF4		
50	VREF3		
51	VREF2		
52	VREF1		
53	NC	No Connection	
54	VON	Gate Driver Power Supply	
55	VOFF	Gate Driver Ground	4)
56	/POL	Polarity Control Input (Invert)	
57	DATA2	Gate Driver Control Input	
58	DATA1		
59	CPV	Gate Shift Clock Input	
60	GND	Ground(0V)	3)

Notes 1) All AVDD pins shall be connected to +12.6V(TBD).

2) All VDD pins shall be connected to +2.5V(Typ.).

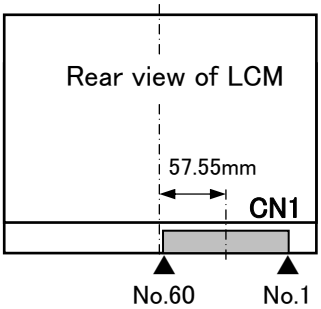
3) All GND pins shall be grounded. Metal bezel is internally connected to GND.

4) All VOFF pins shall be connected to -5.8V(Typ.).

5) LVn+L/R and LVn-L/R (n=0～2) should be wired by side-by-side FPC patterns, respectively.

6) High level as write enable, Low level or open as write protect

7) EEP-ROM device adress: "1010000"



5. 2 Backlight unit

JST BDAMR-02VAS-3(M)

(Matching connector : S02-BDAS-3 (LF)(SN)(B))

PIN No.	SYMBOL	DESCRIPTION	NOTE
1	HV	Power supply (High voltage)	
2	HV	Power supply (High voltage)	

5. 2 Backlight unit

CN1:JST PHR-12

(Matching connector : JST S12B-PH)

PIN No.	DESCRIPTION	NOTE
1	Anode 1	
2	No connection	
3	Cathode 1-1	
4	Cathode 1-2	
5	No connection	
6	No connection	
7	No connection	
8	No connection	
9	Cathode 2-2	
10	Cathode 2-1	
11	No connection	
12	Anode 2	

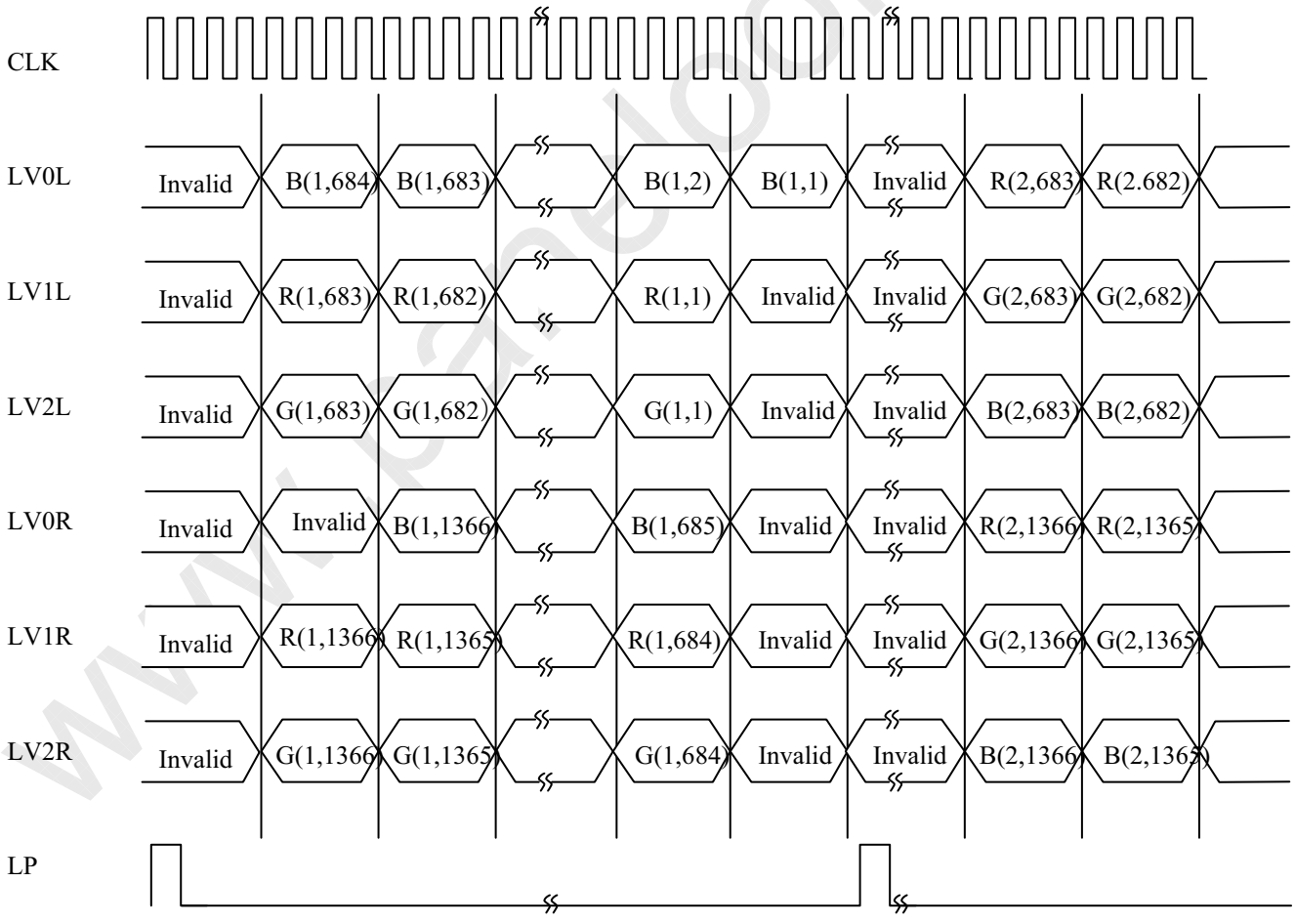
5. 3 Correspondence between input data and display image

Display data of adjacent two pixel is latched during four cycle of CLK.

B (1,1)	G (1,1)	R (1,1)

Pixel : R0 - R7 : R (x,y)
G0 - G7 : G (x,y)
B0 - B7 : B (x,y)

1 , 1	1 , 2	1 , 3	- -	1 , 1366
2 , 1	2 , 2	2 , 3	- -	2 , 1366
3 , 1	3 , 2	3 , 3	- -	3 , 1366
⋮	⋮	⋮		⋮
768 , 1	768 , 2	768 , 3		768 , 1366



5. 4 Relationship between display colors and input signals

Color \ Input		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note 1) Definition of gray scale :

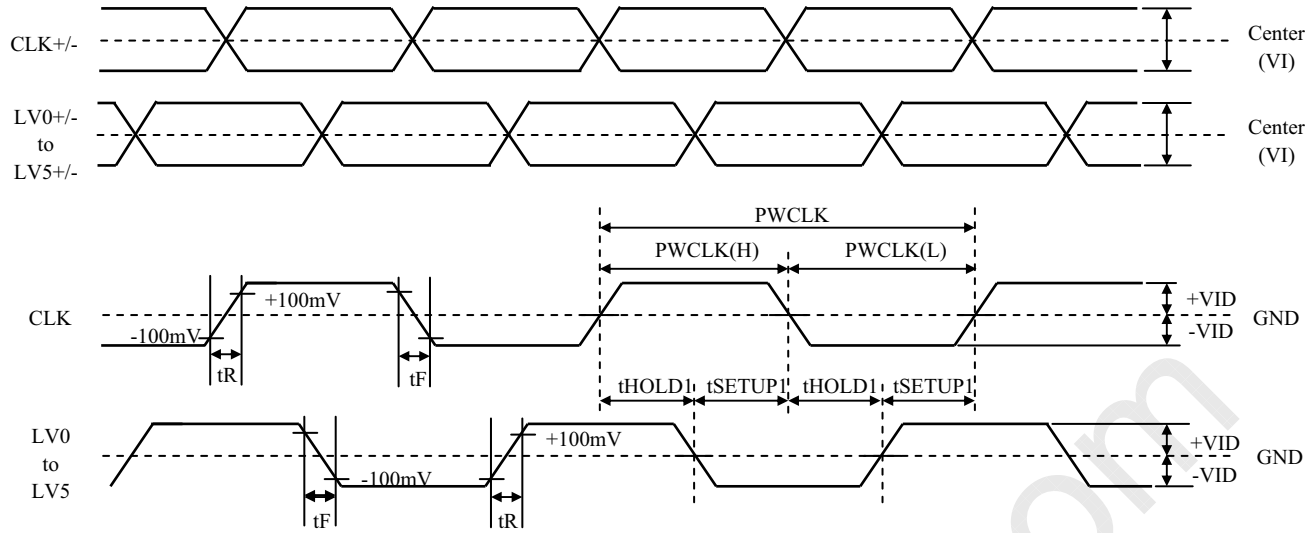
Color(n) · · · Number in parenthesis indicates gray scale level.

Larger n corresponds to brighter level.

2) Data : 1 : High, 0 : Low

6. INTERFACE TIMING

6. 1 mini-LVDS receiver timing



LVn=(LVn+)-(LVn-) n=0～5

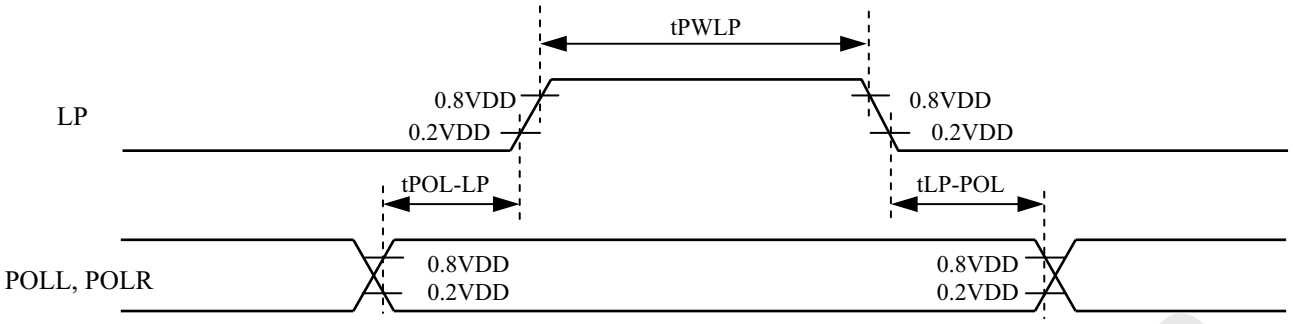
CLK=(CLK+)-(CLK-)

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Clock period	PWCLK	5.9	6.4	7.3	ns	
Clock high level width	PWCLK(H)	2.5	3.2	-	ns	
Clock Low level width	PWCLK(L)	2.5	3.2	-	ns	
Data setup time	tSETUP1	1.0	-	-	ns	
Data hold time	tHOLD1	1.0	-	-	ns	
mini-LVDS rise time	tR	-	-	0.8	ns	
mini-LVDS fall time	tF	-	-	0.8	ns	
mini-LVDS differential voltage	VID	100	-	600	mV	
mini-LVDS common mode input voltage range	VI	0.3+VID/2	-	VDD-1.3 -VID/2	V	

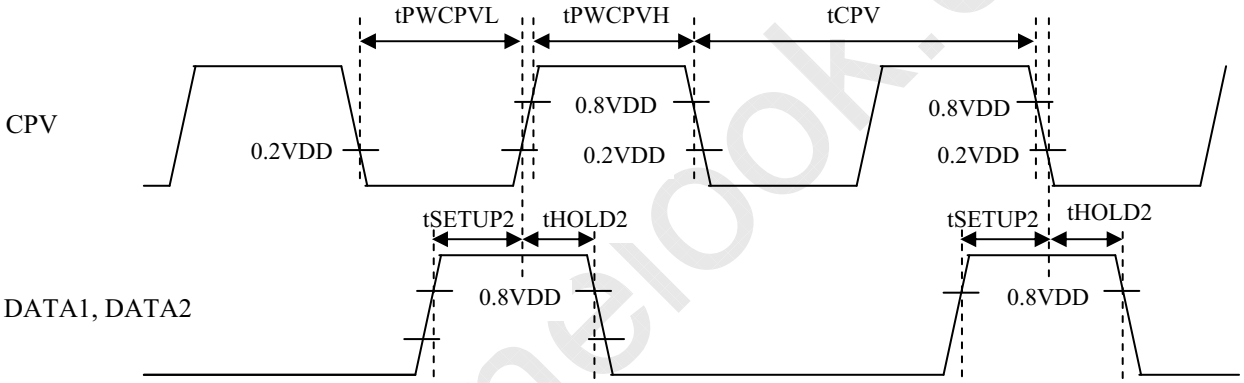
Notes 1) The above specification is defined at each Source Driver IC inputs.

6. 2 Control signal timing

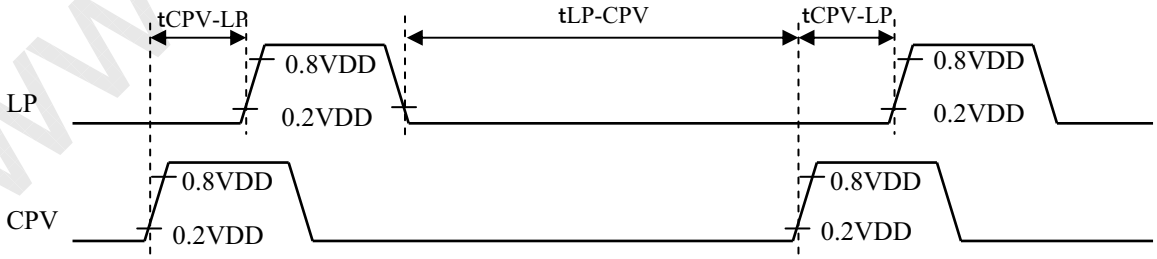
Notes 1) The following specification is defined at connector CN1.



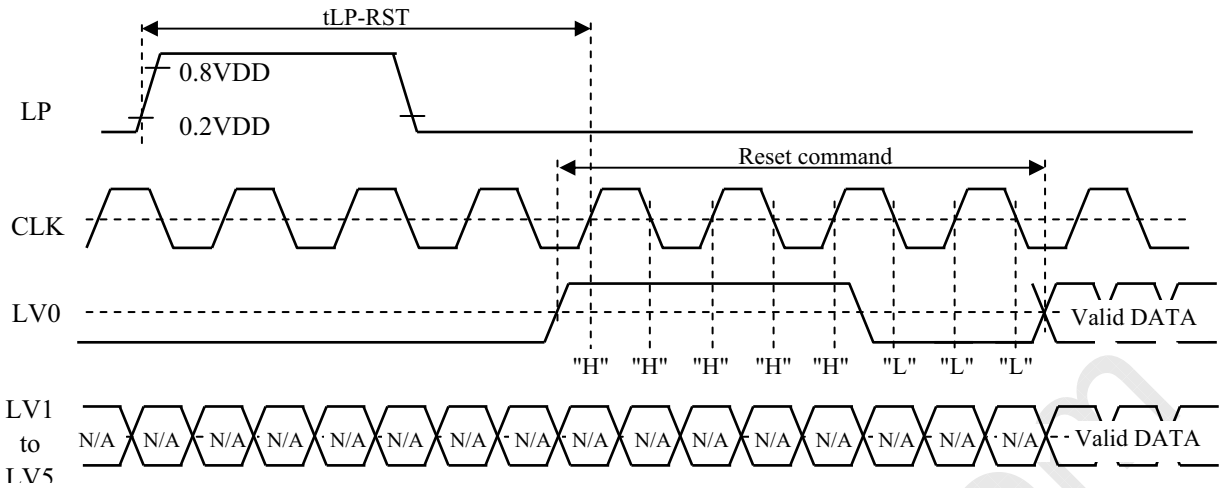
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Latch clock high level width	tPWLP	1500	1580	-	ns	
POL setup time	tPOL-LP	100	-	-	ns	
POL hold time	tLP-POL	100	-	-	ns	



ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Gate shift clock period	tCPV	20	-	-	µs	
Gate shift clock high level width	tPWCPVH	500	-	-	ns	
Gate shift clock low level width	tPWCPVL	500	-	-	ns	
Data setup time	tSETUP2	200	-	-	ns	
Data hold time	tHOLD2	200	-	-	ns	



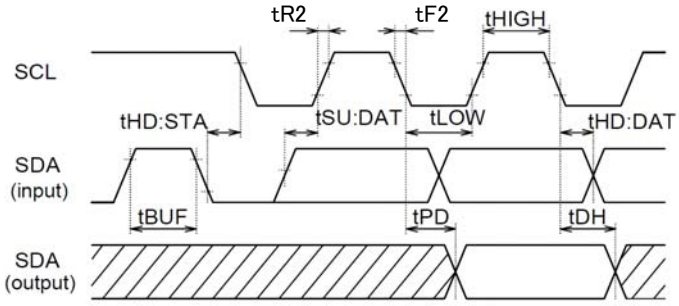
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Gate delay time	tCPV-LP	5.8	-	-	µs	
TFT charge time	tLP-CPV	11	12	-	µs	



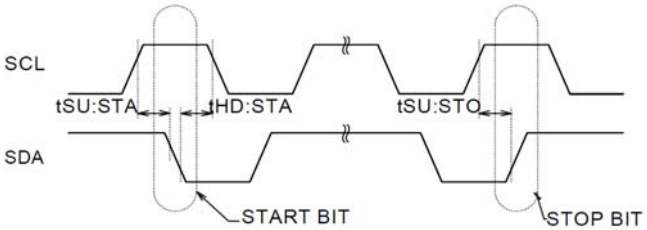
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Reset input time	tLP-RST	500	-	-	ns	

6. 3 I2C BUS timing

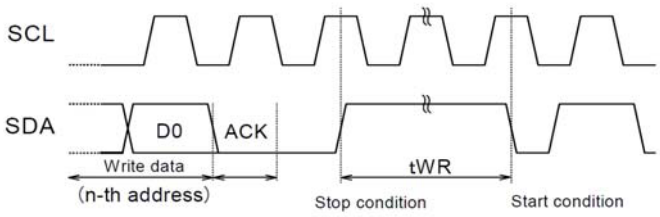
Notes 1) The following specification is defined at connector CN1.



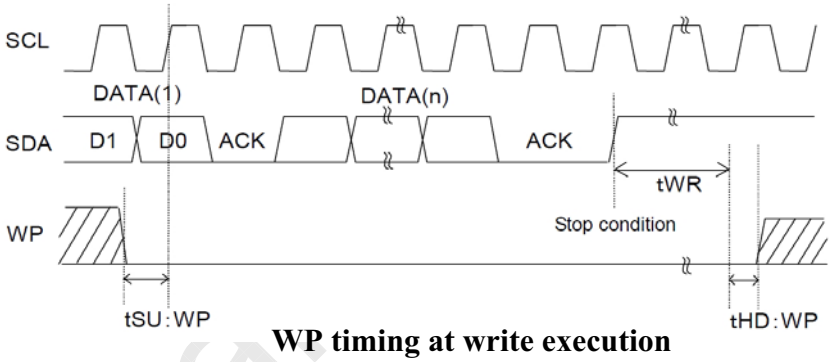
Sync data input/output timing



Start-stop bit timing



Write cycle timing



WP timing at write execution

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
SCL frequency	fSCL	-	-	100	kHz	
Data clock high level width	tHIGH	4.1	-	-	us	
Data clock low level width	tLOW	4.8	-	-	us	
SDA, SCL rise time	tR2	-	-	0.9	us	
SDA, SCL fall time	tF2	-	-	0.2	us	
Start condition hold time	tHD:STA	4.1	-	-	us	
Start condition setup time	tSU:STA	4.8	-	-	us	
Input data hold time	tHD:DAT	50	-	-	ns	
Input data setup time	tSU:DAT	250	-	-	ns	
Output data delay time	tPD	80	-	4000	ns	
Output data hold time	tDH	50	-	-	ns	
Stop condition setup time	tSU:STO	4.1	-	-	us	
Bus release time	tBUF	4.8	-	-	us	
Internal write cycle time	tWR	-	-	11	ms	
WP hold time	tHD:WP	0.1	-	-	ns	
WP setup time	tSU:WP	2.0	-	-	us	

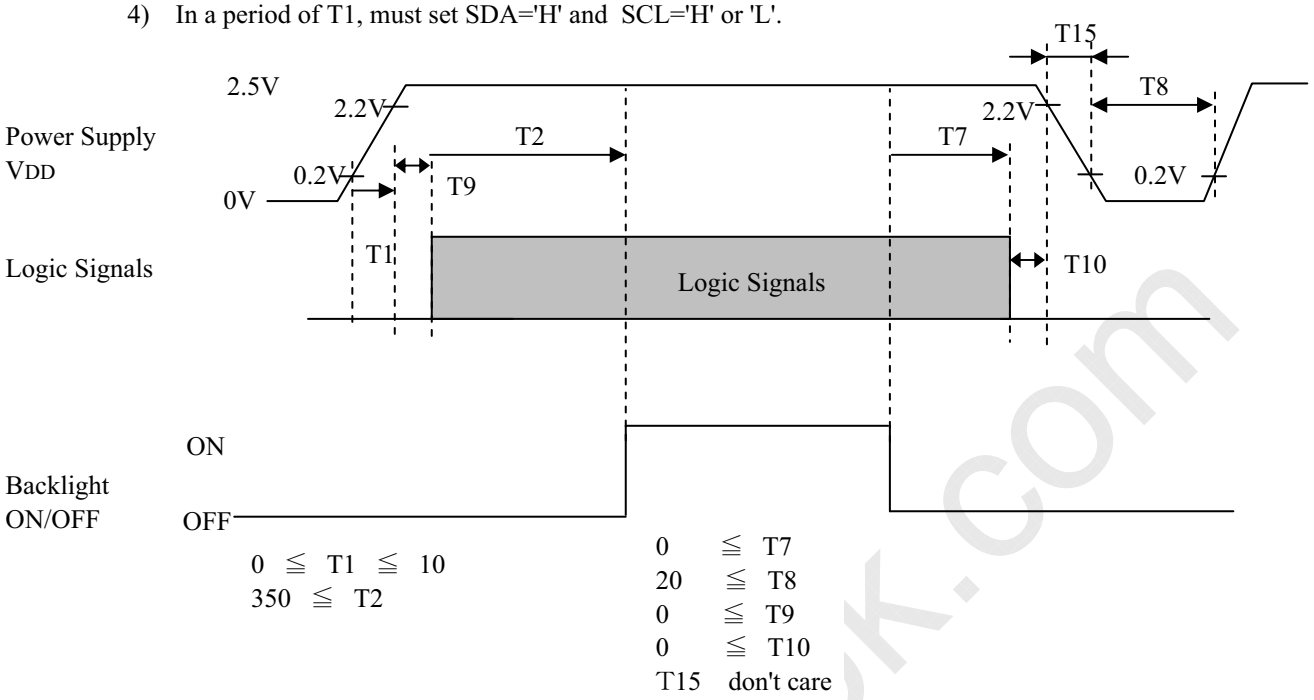
6.4 Timing between interface signals power supply

Notes 1) The following specification is defined at connector CN1.

2) In the T16 and T17, the float equal to or less than 1.5V of AVDD is no object.

3) In the T24 and T25, the float equal to or less than 1.5V of VON is no object.

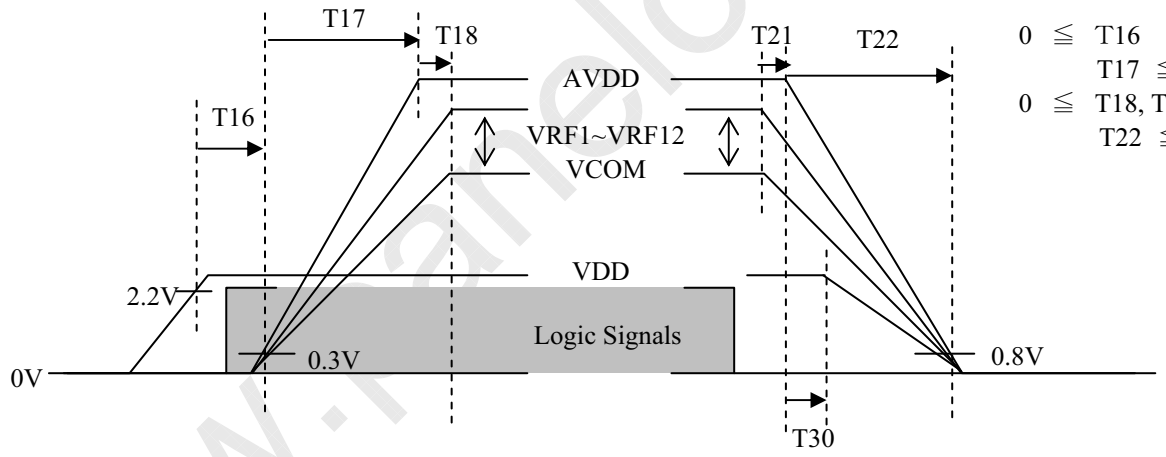
4) In a period of T1, must set SDA='H' and SCL='H' or 'L'.



0 ≦ T1 ≦ 10
350 ≦ T2

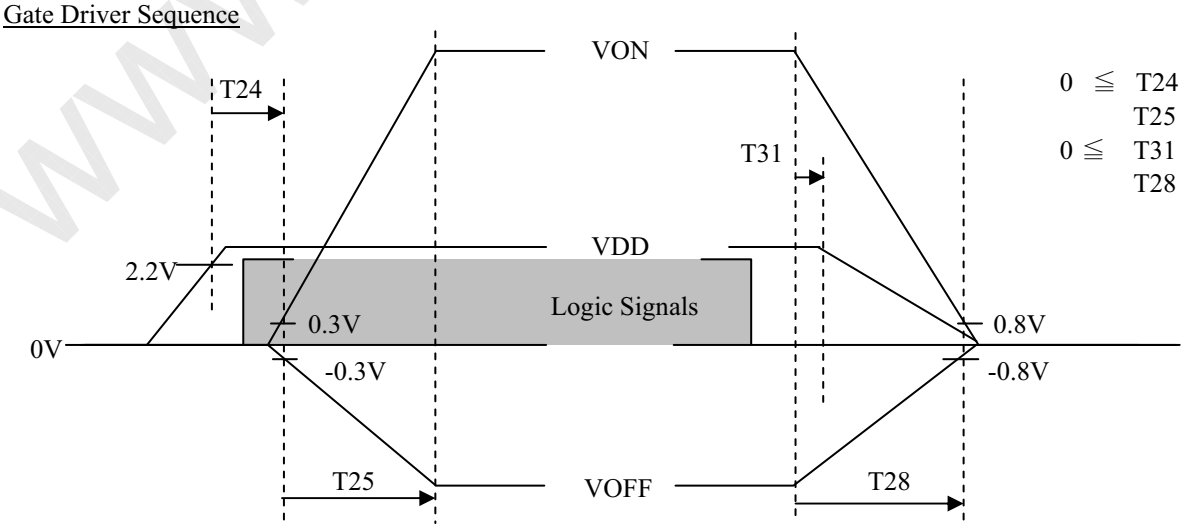
0 ≦ T7
20 ≦ T8
0 ≦ T9
0 ≦ T10
T15 don't care

Source Driver & VCOM Sequence



0 ≦ T16
T17 ≦ 10
0 ≦ T18, T21, T30
T22 ≦ 1000

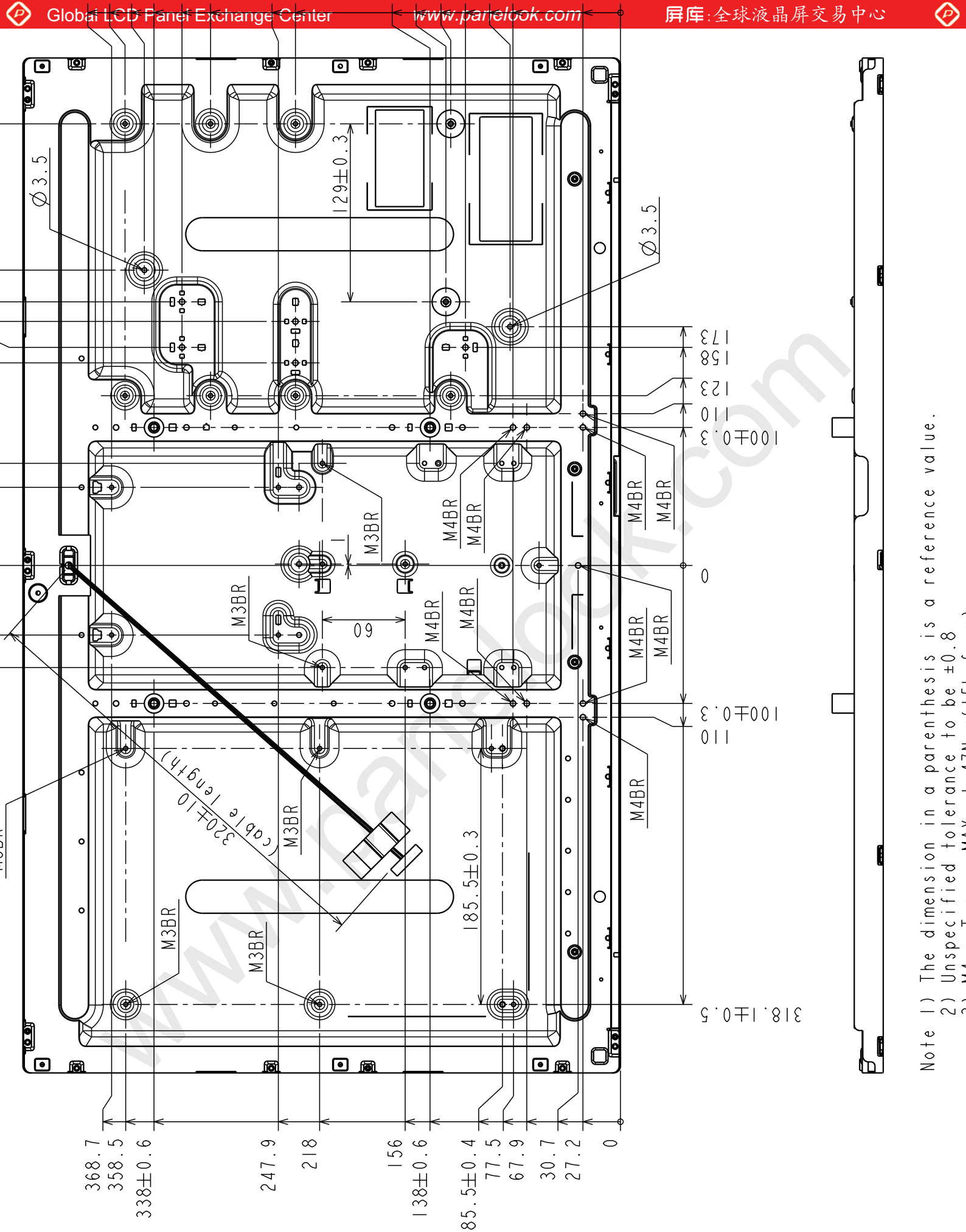
Gate Driver Sequence



0 ≦ T24
T25 ≦ 10
0 ≦ T31
T28 ≦ 1000

Unit : ms

Note 1) The dimension in a parenthesis is a reference value.
2) Unspecified tolerance to be ±0.8



Note 1) The dimension in a parenthesis is a reference value.
2) Unspecified tolerance to be ±0.8